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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/891,885	06/26/2001	Mark T. Ramsbey	F0279	2423

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EXAMINER	
MAGEE, THOMAS J	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/891,885	RAMSBEY ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-13 and 15-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-13 and 15-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections – 35 U.S.C. 103

1.The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higashitani et al. (US 6,448,593 B1) in view of Huang (US 5,378,649).

3. Regarding Claim 9, Higashitani et al. disclose a method of forming a flash (non-volatile) semiconductor memory device, wherein a substrate is provided with a a core and a peripheral region (Col. 1, lines 14 – 40) with one or more insulating regions (Figure 2) for one or more ESD transistors (Col. 1, lines 29 – 40, Col. 2, line 66 through Col. 3, line 7) formed in the periphery region of the flash memory array and poly layers (P1, P2, Figure 2) over the insulating layers. Higashitani et al. disclose that after patterning to form ESD and other transistors, spacers are formed (Col. 3, lines 14 – 19) (Figure 2, 108) subsequent to formation and etching of an oxide layer (106).Further, Higashitani et al. disclose (Col. 3, lines 16 – 19) that heavy (n+) doping is done to form source/drain regions.

Higashitani et al. do not explicitly disclose that word lines in the core region are spaced apart by 1 um or less. Huang discloses that the polycrystalline silicon word lines used in a non volatile memory device are spaced at a distance in the range, 0.1 to 0.5 um, consistent with

the value recited in the instant application. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Higashitani et al. and Huang to obtain poly-silicon word lines at appropriate spacings to reduce crosstalk and coupling.

4. Regarding Claim 10, Higashitani et al. disclose that LDD masks (Figure 2) are done, followed by LDD implants, whereupon, the ESD transistors (select gate) (Col. 4, lines 36 – 39) are formed in a fixed location with spacers formed from an oxide layer (Figure 2, 106) and other areas are "unmasked" (all LDD masks removed) and areas etched (Col. 4, lines 7 – 8) followed by heavy n+ ion implant doping.

5. Claims 11 and 16 are rejected as being unpatentable over Higashitani et al. in view of Huang, as applied to Claims 9 and 10, and further in view of Diaz et al. ("Building-In ESD/EOS Reliability for Sub-Half Micron CMOS Processes," IEEE Trans. on Electron Devices, Vol.43, No. 6, (1996) pp. 991 – 999).

6. Regarding Claims 11 and 16, Higashitani et al. do not disclose the implant dose and species of impurity comprising the heavy doping. Diaz et al. disclose for a MOSFET ESD transistor, similar to the recitation of the instant application (p.3, lines 13 – 20), that the heavy implant (DDD) comprises phosphorus in the dose range,7 x 10 ^ (14) to 10 ^ (15)/cm^(2) at energies in the range, 60 – 65 keV.
Since the FET will function in a memory device (p.3), it would be obvious to one of ordinary skill in the art at the time of the invention to combine Diaz et al. with Higashitani et al. to obtain an optimum implant condition to utilize in the memory device. Further,

although the title of the Diaz et al. reference is directed toward a CMOS process, a preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

7. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higashitani et al. in view of Huang et al., as applied to Claims 9 and 10, and further in view of Reisinger (US 6,137,718).

8. Regarding Claims 12 and 13,Higashitani et al. do not explicitly disclose that the flash memory array is a SONOS type structure, but this would have been an easy modification. SONOS cells have been present since the late 1960's. Reisinger discloses (Col. 8, lines 5 12) the formation of MOS transistors with multi-layer dielectrics (51,52,53) capped by a polysilicon layer (6) (See Figure 1) to produce a classical SONOS structure for a non-volatile memory cell. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to add Reisinger to Higashitani et al. to obtain a SONOS structure with improved dielectric properties and increased storage density in the memory circuit (Reisinger, Abstract).

9. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Higashitani et al. in view of Huang et al., as applied to Claims 9 and 10, and further in view of Shiue et al. (US 5,953,601).

Higashitani et al. do not disclose masking of the core region when heavily doping the source/ drain regions of the ESD transistors. Shiue et al. disclose (Col. 4, lines 34 – 49) heavy ion implantation of source/drain regions of ESD transistors (100) (Figure 2b) while masking the core region (200) (internal region). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the procedures of Shiue et al. in Higashitani et al. to produce heavily doped regions without damaging adjacent regions.

10. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higashitani et al. in view of Huang et al., as applied to Claims 9 and 10, and further in view of Diaz et al.

11. Regarding Claims 17 and 18,Higashitani et al. disclose a method of forming a flash (non-volatile) semiconductor memory device, wherein a substrate is provided with a core and a peripheral region (Col. 1, lines 14 – 40) with one or more insulating regions (Figure 2) for one or more ESD transistors (Col. 1, lines 29 – 40, Col. 2, line 66 through Col. 3, line 7) formed in the periphery region of the flash memory array and poly layers (P1, P2, Figure 2) over the insulating layers.
Higashitani et al. disclose that after patterning to form ESD and other transistors, spacers are formed (Col. 3, lines 14 – 19) (Figure 2, 108) subsequent to formation and etching of an oxide layer (106). Further, Higashitani et al. disclose (Col. 3, lines 16 – 19) that heavy (n+) doping is done to form source/drain regions.

Higashitani et al. do not explicitly disclose that word lines in the core region are spaced apart

by 1 um or less. Huang discloses that the polycrystalline silicon word lines used in a non volatile memory device are spaced at a distance in the range, 0.1 to 0.5 um, consistent with the value recited in the instant application. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Higashitani et al. and Huang to obtain poly-silicon word lines at appropriate spacings to reduce crosstalk and coupling.

Higashitani et al. do not disclose the implant dose and species of impurity comprising the heavy doping or light drain doping (LDD). Diaz et al. disclose for a MOSFET ESD transistor, similar to the recitation (p.3, lines 13 – 20) of the instant application, that the LDD implant comprises phosphorus in the dose range, 8 x 10^ (13) to 10^(14)/cm^(2) in the energy range, 50 to 65 keV and the (P) heavy implant (DDD) is in the dose range, 7 x 10 ^ (14) to 10 ^ (15)/cm^(2) at energies in the range, 60 – 65 keV. Since the FET will function in a memory device (p.3), it would be obvious to one of ordinary skill in the art at the time of the invention to combine Diaz et al. with Higashitani et al. to obtain optimum implant conditions to utilize in the memory device. Further, although the title of the Diaz et al. reference is directed toward a CMOS process, a preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Conclusions

12. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(703) 305 5396.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Tom Thomas**, can be reached on **(703) 308-2772.**. The fax number for the organization where this application or proceeding is assigned is **(703) 308-7722.**

URI NADAV
patent examiner

Thomas Magee
September 21, 2003